Please replace the paragraph on page 6, lines7-9, with the following revised paragraph:

--FIGS. 3a through 3d, schematically illustrate a series of cross-sectional representations which illustrate the progressive stages in completing the fabrication of a FET device in accordance with a process of the present invention.--

Please replace the paragraph on page 8, starting at line 4 with the following revised paragraph:

--Generally, although not necessary for the practice of the invention, further materials may be deposited to form additional material layers upon the polysilicon layer 18 of the gate electrode 16. The typical materials of these layers include metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks), which are used with the purpose to improve the electrical characteristics of the device. In a preferred embodiment, a relatively thin layer of titanium nitride (TiN) is deposited on the polysilicon layer 18 to form a barrier layer 20. The barrier layer 20 is then blanketed with a tungsten (W) layer 22 to complete the formation of the gate electrode 16.--

Please replace the paragraph on page 12, starting at line 2 with the following revised paragraph:

--In forming the source/drain regions 28a and 28b, a first ion implantation is made using the gate electrode 16 and the field isolation regions 12 to mask the substrate, in order to form the more lightly doped portions of LDD source/drain regions 30a and 30b. Generally, although not necessary for the practice if the invention, as shown by FIG. 3c, provided on both sides of the gate electrode 16 are electrode spacers 32. The electrode spacers 32 may be formed from materials including but not limited to insulating materials such as silicon oxides, silicon nitrides and silicon oxynitrides. Various processes are used to form electrode spacers 32. Such processes include Reactive Ion Etch (RIE), and the

above mentioned material deposition methods. Typically, electrode spacers 32 are formed by depositing an oxide film, such as tetraethoxysilane (TEOS) oxide at between about 600 to about 720 degrees centigrade to a thickness of between about 300 Å to about 700 Å. A second ion implantation is performed to complete the source/drain regions 28a and 28b with HDD source/drain regions 34a and 34b. In the illustrated FET device 2, the source/drain regions 28a and 28b may be doped with any n-type or p-type dopant or combinations of different n-type dopants or p-type dopants might be used to achieve different diffusion profiles. Further, it is to be appreciated that the angled ion implantation step of the present invention, if desired, could be carried out at this stage in the fabrication of the FET device 2, as there are no apparent advantages or disadvantage in performing this step before or after the formation of either the LDD, the spacers, or even the HDD.--

Please insert the following paragraph on page 15, between lines 7 and 8:

--For example, FIG. 3E illustrates a circuit structure comprising a semiconductor layer 10 and a first dopant-type MOS transistor 2a situated on the semiconductor layer 10 having a source region 28a and a drain region 28b in the semiconductor layer 10 which are doped with a first conductivity-type dopant 37a, a channel region 29 located between the source/drain regions 28a and 28b, a gate oxide layer 14a located on a surface of the channel region 29, and a gate electrode 16a located on the gate oxide layer 14a. The portion of the gate oxide layer 14a, which is beneath the gate electrode 16a and adjacent the drain region 28b and which defines an overlap region 26a, has an ion implant concentration which is effective to lower the surface electrical field in the overlap region 26a. A second-type dopant MOS transistor 2b, which is complementary to the first dopant-type MOS transistor 2a, is situated on the semiconductor layer 10 and includes a second gate oxide layer 14b, two complementary source/drain regions 28c and 28d, which are doped with a second conductivity-type dopant 37b, and a complementary gate electrode 16b located on the second gate oxide layer 14b. Additionally, a portion of the second gate oxide layer 14b, which is beneath the complimentary gate electrode 16b and adjacent the complimentary drain region 28d and which defines a second overlap region

26b, has an ion implant concentration which is effective to lower the surface electrical field in the second overlap region 26b. Preferably, the ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.--

Please replace the Abstract, with the following amended abstract:

--An integrated circuit which provides a FET device having reduced GIDL current is described. A semiconductor substrate is provided wherein active regions are separated by an isolation region and a gate oxide layer is provided on the active regions. A gate electrode is provided upon the gate oxide layer wherein beneath an edge of the gate electrode, a gate-drain overlap region having a high dose ion implant is provided.--

In the Claims

The entire set of presently pending claims has been reproduced below for the convenience of the Examiner. Amended claims and new claims are indicated as such in the parenthetical following each claim number.

1. (Amended) A circuit structure comprising:

a semiconductor layer;

an oxide layer formed on said semiconductor layer;

a gate structure formed on said oxide layer having a defined leading edge; and

an overlap region beneath said gate structure and adjacent said leading edge having a predetermined ion implant concentration higher than adjacent oxide layer portions, said predetermined implant concentration being sufficient to increase the electrical gate oxide thickness in said overlap region.

2. The circuit structure according to claim 1, wherein said predetermined ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.